

Special Shoutout to KESBACH1 for scanning his Clean Sweep schematics for all to see!

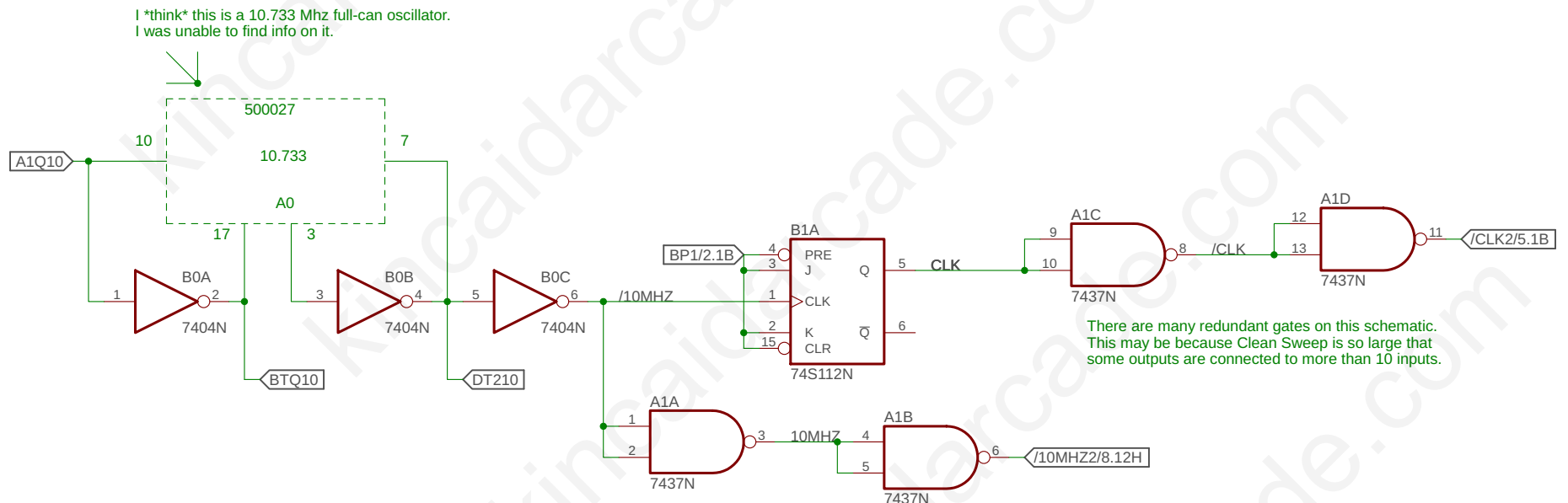
Find them at mameworld.info

<http://mameworld.info/ubbthreads/showflat.php?Cat=&Number=315375&page=8&view=expanded&sb=7&o=&vc=1>

Redrawn by Alexander Haley  
KincaidArcade

kincaidarcade.com

SCHEMATIC CONTAINS ERRORS.  
USE AT OWN RISK.



TITLE: Clean Sweep REV-D ETR

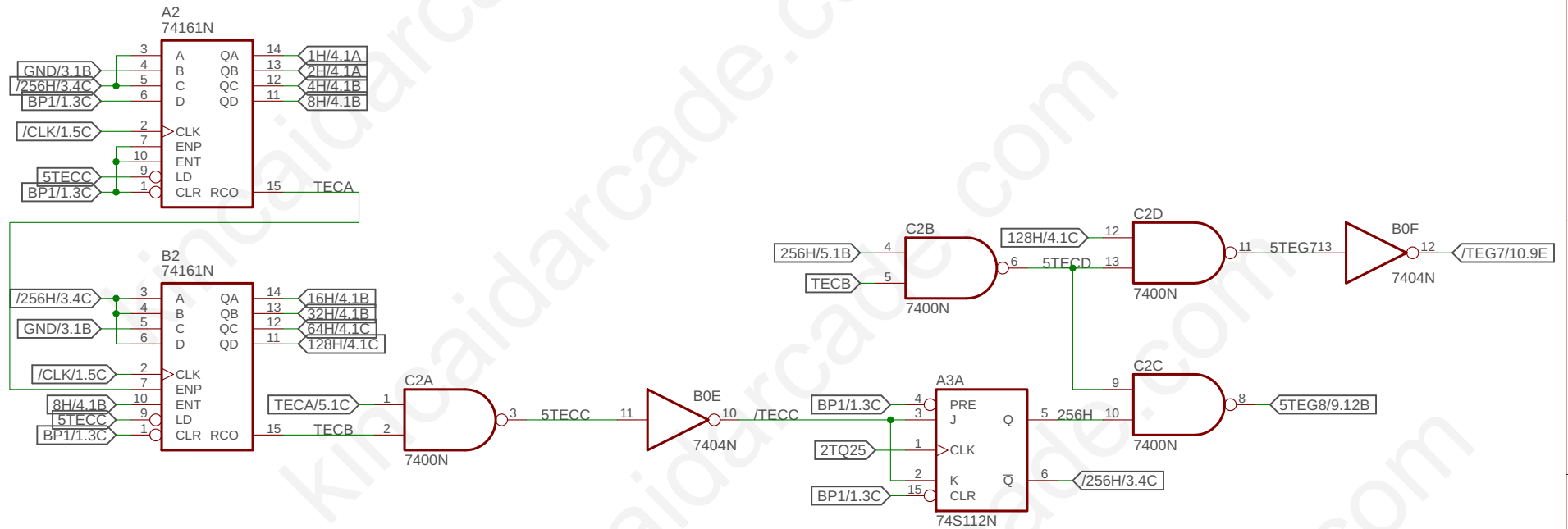
Document Number:

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# This is the Horizontal Sync Generator:



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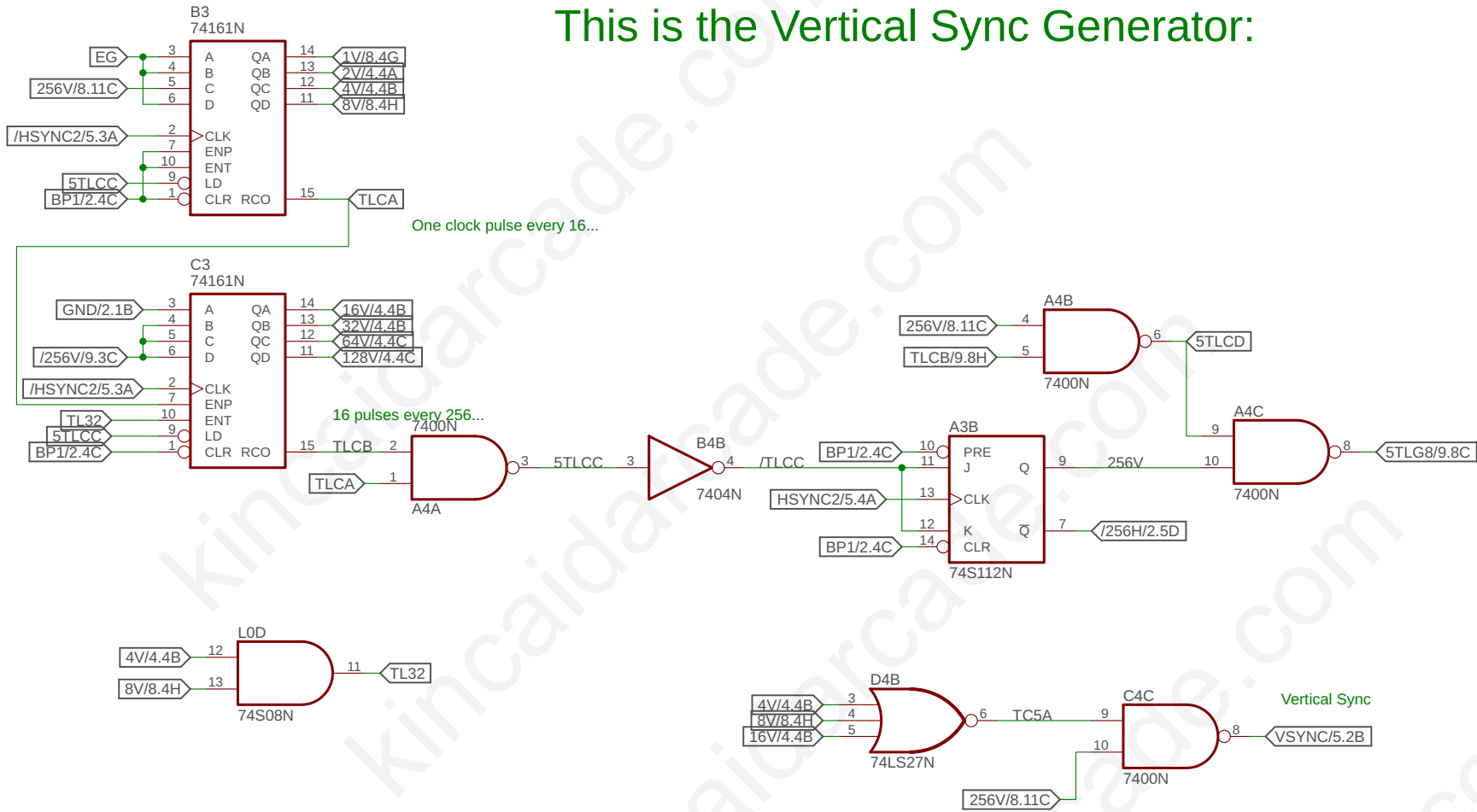
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# This is the Vertical Sync Generator:



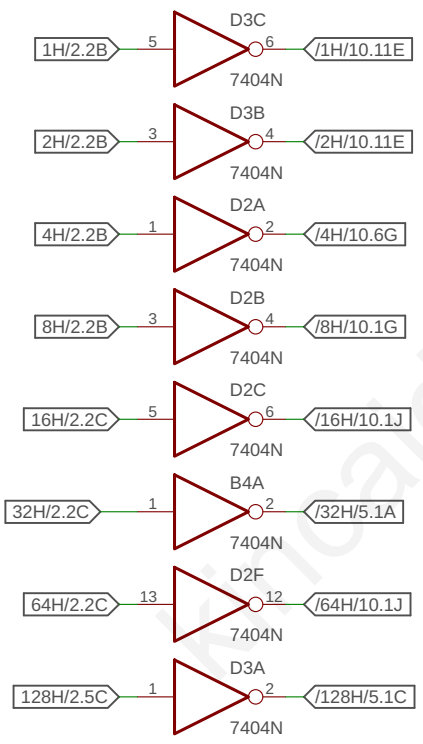
TITLE: Clean Sweep REV-D ETR

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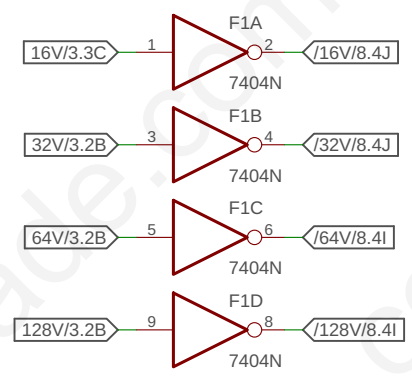
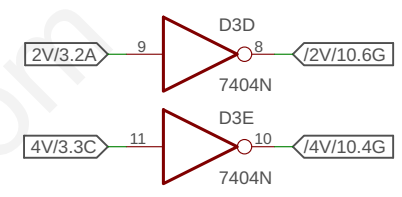
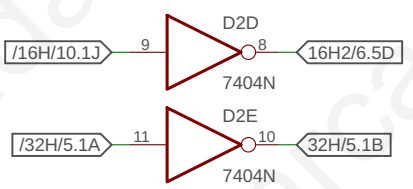
REV:

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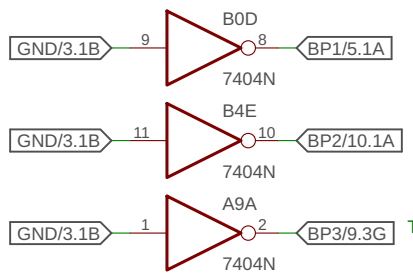
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I think RAMTEK has these redundant gates because they need to have a signal drive more inputs than the output can handle. (I.E. more than 10 LSTTL inputs.)



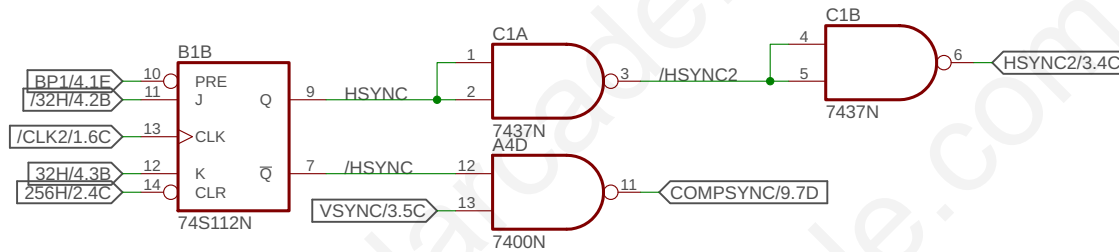
"BP" stands for "Buffered Pullup"  
 MEANING: An inverter has had its input connected to ground, and the output is ~5 volts, the equivalent of what a pullup resistor does.



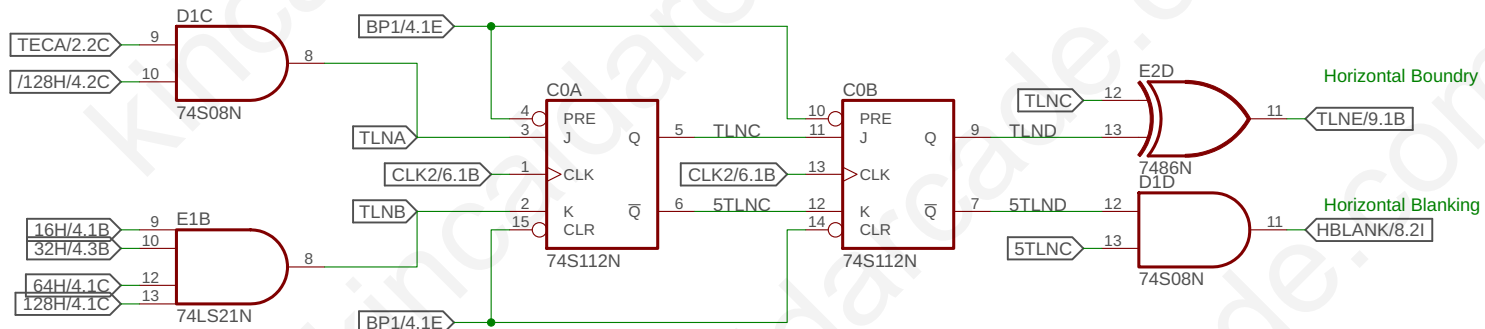
The pins on this gate were not labeled...

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# Video Sync Generation:

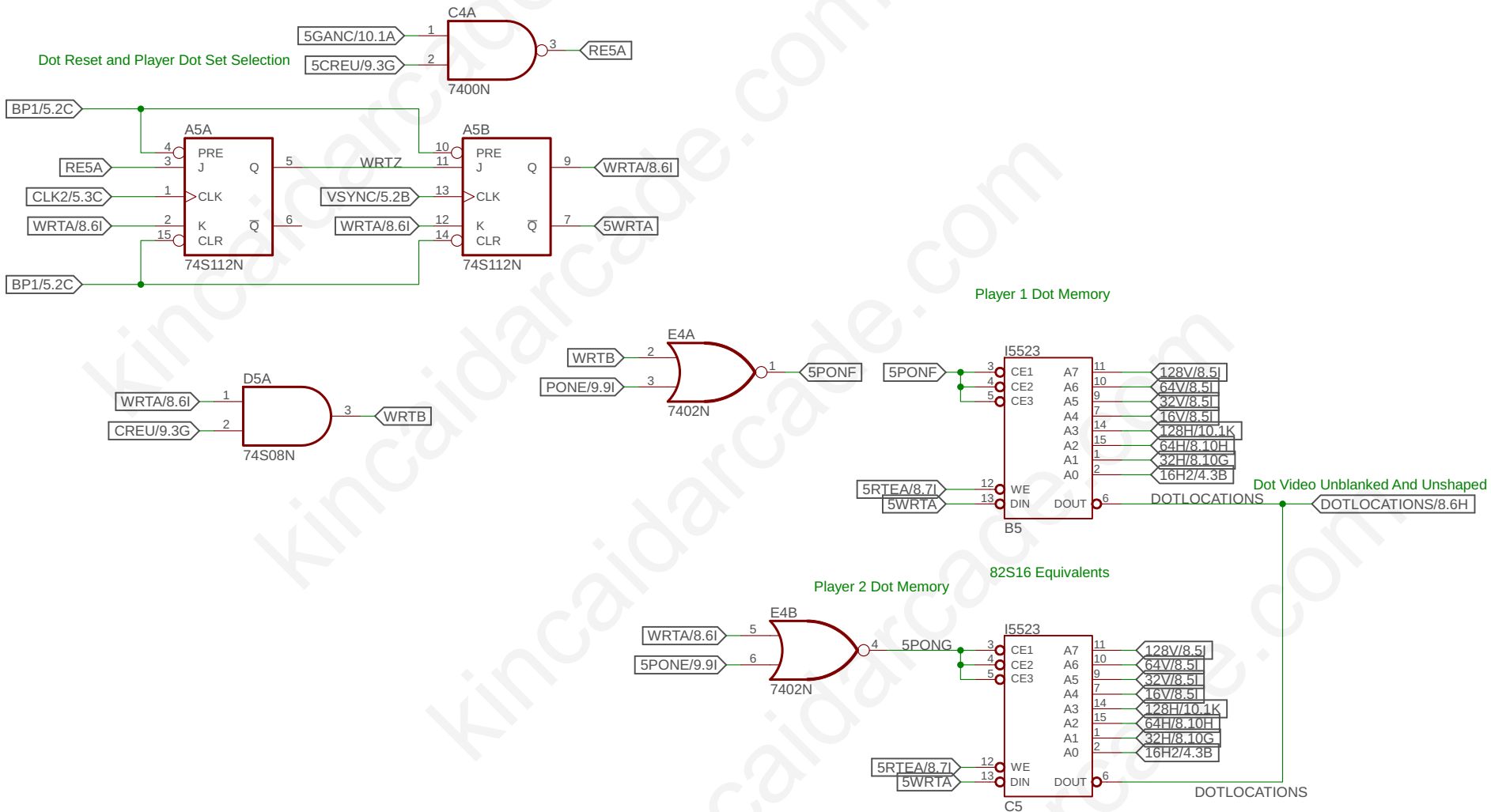


## Horizontal Boundary and Blanking



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# Dot Memory



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1

2

3

4

5

6

A

B

C

D

E

A

B

C

D

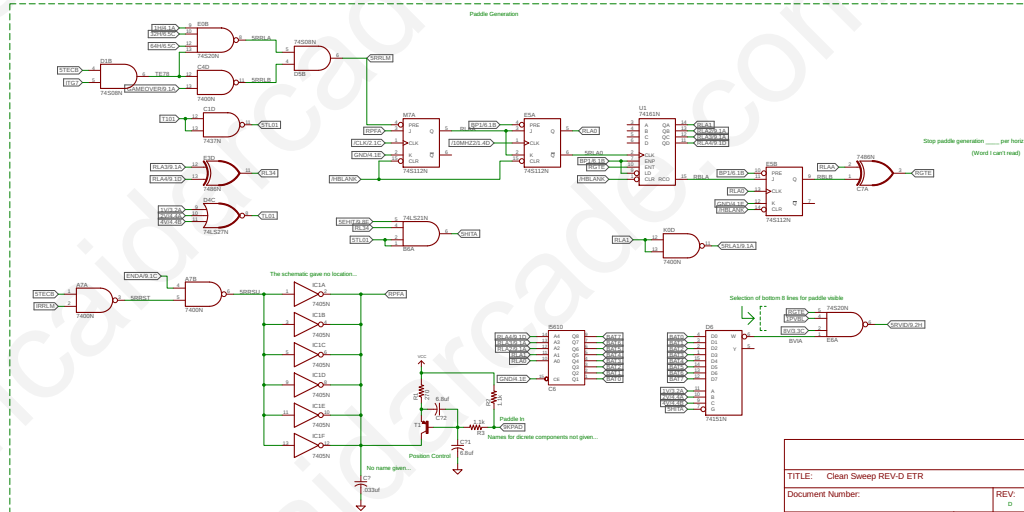
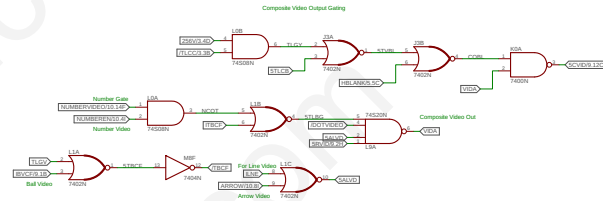
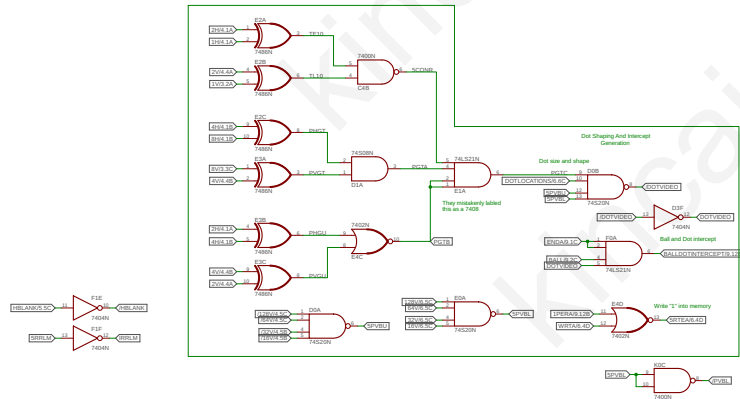
E

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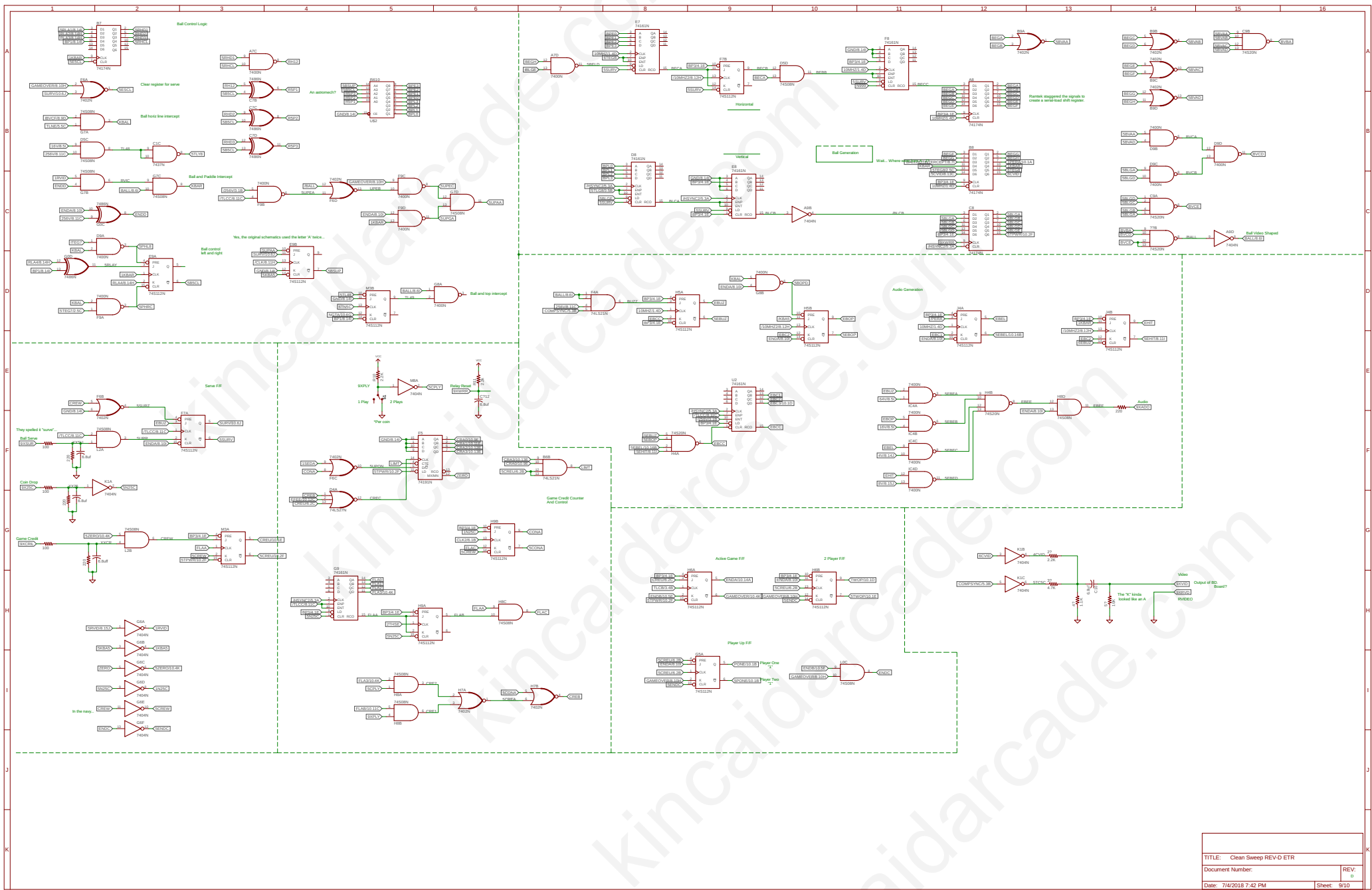
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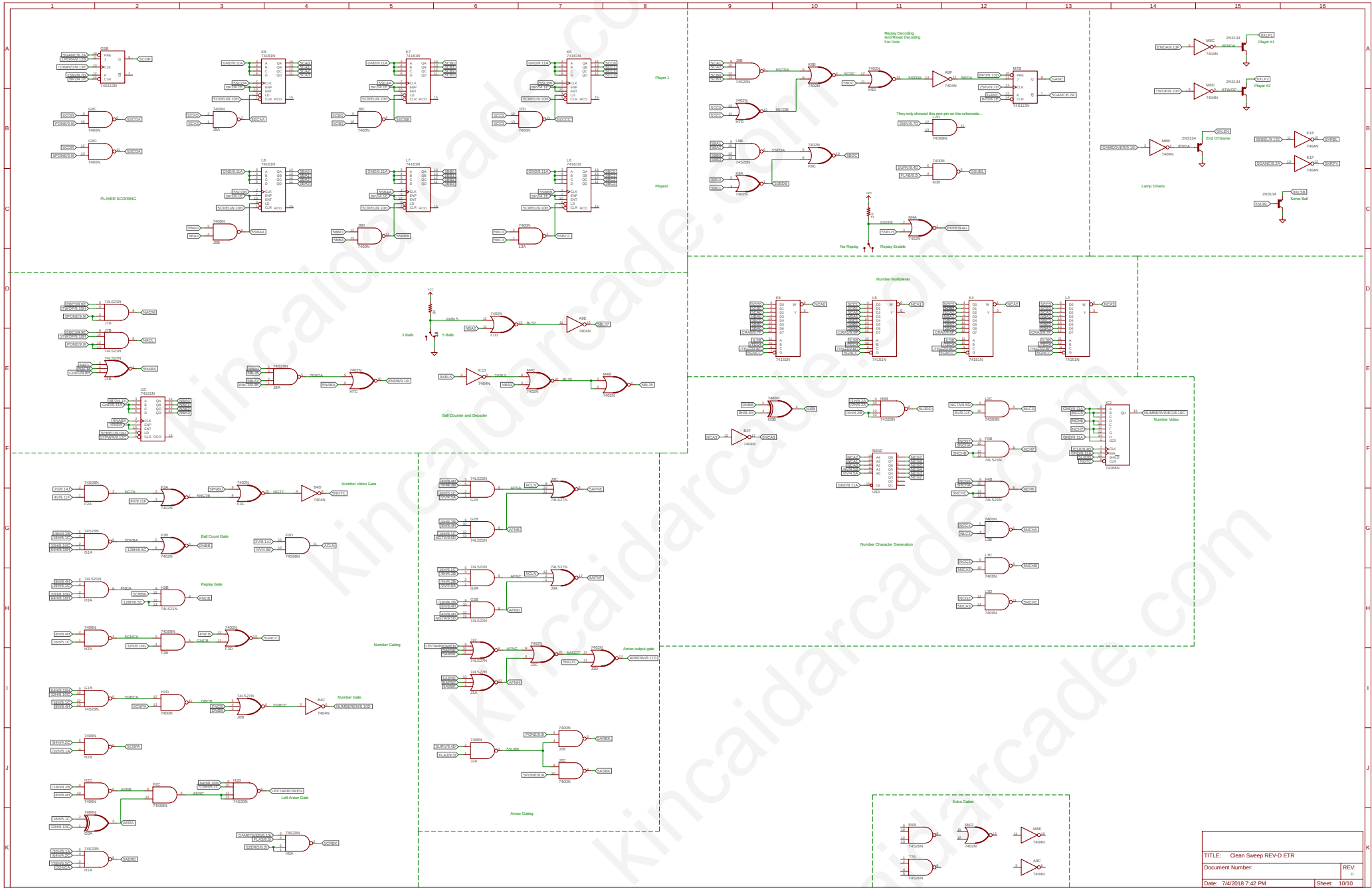
SCHEMATICS REDRAWN BY ALEXANDER OF KINCAID ARCADE  
 (A 15 Year Old!)



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